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10/634,867

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Hyang-Shik Kong

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01/27/2005

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EXAMINER

DUONG, KHANH B

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/634,867

Applicant(s)

KONG ET AL.

Examiner

Khanh Duong

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 December 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4-7,13,16-22 and 24-33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4-7,13,16-22 and 24-33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 August 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

This Office Action is in response to the Amendment filed on December 22, 2004.

Accordingly, claims 1 and 4 were amended.

Currently, claims 1, 4-7, 13, 16-22 and 24-33 are pending in the application.

Response to Arguments

Applicant's arguments with respect to the amended claims have been considered but are moot in view of the new ground(s) of rejection.

Specification

The disclosure is objected to because of the following informalities: the specification does not describe "depositing an indium zinc oxide (IZO) on the gate insulating layer" as required by claim 13 (line 10).

Appropriate correction is required.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the step of "depositing an indium zinc oxide (IZO) on the gate insulating layer", as required by claim 13 (line 10), must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a

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drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 13 is objected to because of the following informalities: line 9, after "exposing", "the gate" should be --the gate wire-- or --the gate pad--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 and 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko et al. (US 6,433,842) in view of Fogarty et al. (US 4,181,564).

Kaneko et al. ("Kaneko") discloses in FIG. 1 a method for manufacturing a wire contact structure, comprising steps of: forming a wire 8 made of an aluminum-based material; depositing a silicon nitride layer on the wire 8 at a temperature of 230°C to form an insulating layer 10; forming a contact hole 19 extending through the insulating layer 10 and exposing the wire 8; and forming a conductive layer 11 formed of indium tin oxide (ITO) or indium zinc oxide (IZO) and electrically connected to the wire 8 through the contact hole 19.

Re claims 1, 4 and 5, Kaneko discloses depositing the silicon nitride insulating layer 10 at a temperature of 230°C instead of between about 280°C and about 400°C for about 5 minutes to about 40 minutes. Kaneko also fails to disclose the contact hole having a size between about 0.5 mm x 15 µm and 2 mm x 60 µm.

Fogarty et al. ("Fogarty") suggests forming a silicon nitride layer at a temperature between 270°C and 375°C and for a period of about 45 minutes [see col. 2, ln. 65 to col. 3, ln. 3 and col. 4, ln. 35-55].

Since Kaneko and Fogarty are both from the same field of endeavor, the purpose disclosed by Fogarty would have been recognized in the pertinent prior art of Kaneko.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Kaneko as suggested by Fogarty, since Fogarty states at column 4, lines 26-29 such modification would provide a silicon nitride layer having an essentially constant Si/N ratio throughout the thickness of the layer.

Furthermore, with respect to process parameters such as temperature, time and size, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the process parameters within the ranges as claimed, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Re claims 6 and 7, since the contact structure of the wire of Kaneko are formed of the same materials as the claimed invention, it should be inherent that a contact resistance between the aluminum-based material and the IZO is less than 10% of a wire resistance of the wire or less than $0.15 \mu\Omega\text{cm}^2$.

Claims 13 and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song et al. (US 6,163,356) in view of Kaneko and Fogarty.

Song et al. ("Song") discloses in FIG. 4a to 4f a method for manufacturing a thin film transistor array panel, comprising steps of: forming a gate wire formed of an aluminum-based material on a substrate, the gate wire comprising a gate line 13, a gate electrode 11 and a gate pad 15; depositing a silicon nitride layer to form a gate insulating layer 17; forming a semiconductor layer 33 on the gate insulating layer 17; forming a data wire including a data line 23, a source electrode 21, a drain electrode 31 and a data pad 25; forming a passivation layer 37 over the gate insulating layer 17 and the data wire; forming a contact hole 59 extending through the passivation layer 37 and the gate insulating layer 17 and exposing the gate pad 15; depositing an ITO layer over the passivation layer 37; and patterning the ITO layer to form: a redundant gate pad 57 connected to the gate pad 15 through the contact hole 59, a pixel electrode connected

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to the drain electrode 31, and a redundant data pad 67 connected to the data pad 25 [see col. 4, ln. 30 to col. 5, ln. 67].

Re claims 13 and 18-22, Song fails to disclose the following: depositing the silicon nitride gate insulating layer at a temperature between about 280°C and about 400°C, and depositing an indium zinc oxide (IZO) layer over the passivation layer 37.

Fogarty suggests forming a silicon nitride layer at a temperature in the range of 270-375°C for a period in the range of about 45 minutes [see col. 2, ln. 65 to col. 3, ln. 3 and col. 4, ln. 35-55]. Kaneko suggests in FIG. 1 depositing either an indium tin oxide (ITO) layer or an indium zinc oxide (IZO) layer over the passivation layer 10 so as to form a pixel electrode 11.

Since Song, Fogarty and Kaneko are from the same field of endeavor, the purpose disclosed by Fogarty and Kaneko would have been recognized in the pertinent prior art of Song.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Song as suggested by Fogarty, since Fogarty states at column 4, lines 26-29 such modification would provide a silicon nitride layer having an essentially constant Si/N ratio throughout the thickness of the layer. In addition, because ITO and IZO were art-recognized equivalent materials as demonstrated by Kaneko at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute one material for the other.

Furthermore, with respect to process parameters such as temperature, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the process parameters within the ranges as claimed, since it has been held that where the general conditions

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of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Claims 16, 17, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song, Fogarty and Kaneko as applied to claims 13 and 18-22 above, and further in view of Arai et al. (US 6,399,222).

Re claims 16, 17, 24 and 25, Song, Fogarty and Kaneko fail to disclose the indium zinc oxide is formed by sputtering target including In_2O_3 and ZnO , wherein the content of Zn in a compound of In_2O_3 and ZnO is in the range of 15-20%.

Arai et al. ("Arai") suggests the indium zinc oxide is preferably formed by sputtering target including In_2O_3 and ZnO , wherein the content of Zn in a compound of In_2O_3 and ZnO is in the range of 1-20% [see col. 4, ln. 22-32].

Since Song, Fogarty, Kaneko and Arai are both from the same field of endeavor, the purpose disclosed by Arai would have been recognized in the pertinent prior art of Song, Fogarty and Kaneko.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined process of Song, Fogarty and Kaneko as suggested by Arai, since Arai states at column 4, lines 47-49 that such modification would provide an electrode layer having a sufficient thickness.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the content of Zn in a compound of In_2O_3 and ZnO within the range as taught by Arai, since it has been held that where the general conditions of a claim are

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disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 4-7, 13, 16-22 and 24-33 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-31 of U.S. Patent No. 6,287,899 in view of Kaneko and Fogarty.

The claims of U.S. Patent No. 6,287,899 ("the U.S. Patent") recite a method for manufacturing a wire contact structure substantially the same as the claims of the instant application. However, the U.S. Patent fails to recite the following: depositing a silicon nitride gate insulating layer at a temperature between about 280°C and about 400°C, and depositing an indium zinc oxide (IZO) layer over the passivation layer 37.

Fogarty suggests forming a silicon nitride layer at a temperature in the range of 270-375°C for a period in the range of about 45 minutes [see col. 2, ln. 65 to col. 3, ln. 3 and col. 4, ln. 35-55]. Kaneko suggests in FIG. 1 depositing either an indium tin oxide (ITO) layer or an indium zinc oxide (IZO) layer over the passivation layer 10 so as to form a pixel electrode 11.

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Since the U.S. Patent, Fogarty and Kaneko are from the same field of endeavor, the purpose disclosed by Fogarty and Kaneko would have been recognized in the pertinent prior art of the U.S. Patent.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of the U.S. Patent as suggested by Fogarty, since Fogarty states at column 4, lines 26-29 such modification would provide a silicon nitride layer having an essentially constant Si/N ratio throughout the thickness of the layer. In addition, because ITO and IZO were art-recognized equivalent materials as demonstrated by Kaneko at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute one material for the other..

Furthermore, with respect to process parameters such as temperature, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the process parameters within the ranges as claimed, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

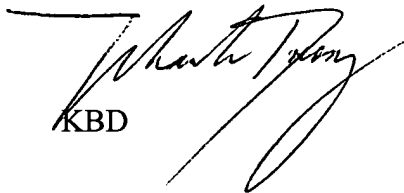
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on Monday - Thursday (9:00 AM - 6:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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